A. Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1.(Currently Amended) A computer system comprising:

a memory system where at least some of the memory is designated as shared memory;

a transaction-based bus ~~mechanism~~ coupled to the memory system wherein the transaction-based bus ~~mechanism~~ includes a cache coherency transaction defined within its transaction set;

a processor having a cache memory, the processor coupled to the memory system through the transaction based bus ~~mechanism~~;

a plurality of system components other than the processor coupled to the transaction-based bus ~~mechanism~~, wherein the system ~~devices~~ components access ~~main~~ the memory system directly through the transaction based bus ~~mechanism~~, but do not access the cache memory directly through the transaction based bus ~~mechanism~~;

a request issued by one of the plurality of system components and addressed to the processor, wherein the request indicates a request to perform a cache coherency operation; and

wherein the processor is configured to respond to the request by treating the request as an explicit command to perform the cache coherency operation.

2.(Previously Presented) The computer system of claim 1 wherein the request is implemented independent of any interrupt mechanism in the processor.

3.(Previously Presented) The computer system of claim 1 wherein the processor response to the request comprises executing the cache coherency operation without the assistance of instructions executed on the processor.

4.(Previously Presented) The computer system of claim 1 wherein the processor is further configured to respond to the request by generating a response message addressed to the system component that initiated the ~~first~~ request indicating status of the cache coherency operation.

5.(Previously Presented) The computer system of claim 1 wherein the cache coherency transaction comprises a cache flush transaction and the request includes an address in the shared memory to be flushed from the cache.

6.(Currently Amended) The computer system of claim 5 wherein the processor is configured to respond to the request by:

looking up the address in the cache;

when the lookup yields a miss, or a hit to a cache line that is unmodified with regard to the main memory system, the processor issues a response to the request immediately;

when the lookup yields a hit to a cache line that is modified with regard to main memory, the processor causes a writeback of the specified line to main memory followed by a response to the request addressed to the system component that generated the request.

7.(Previously Presented) The computer system of claim 1 wherein the cache coherency transaction comprises a cache purge transaction and the request includes an address in the shared memory to be purged from the cache.

8.(Currently Amended) The computer system of claim 7 wherein the processor is configured to respond to the request by:

looking up the address in the cache;

when the lookup yields a miss the processor issues a response to the ~~first~~ request;

when the lookup yields a hit to a cache line that is modified with regard to the ~~main~~ memory system, the processor causes a writeback of the specified line to the ~~main~~ memory system followed by an invalidation of the cache line and a

response to the request addressed to the system component that generated the request; and

when the lookup yields a hit to a cache line that is not modified with regard to the ~~main~~ memory system, the processor causes an invalidation of the cache line and a response to the request addressed to the system component that generated the request.

9. (Previously Presented). A method for managing cache coherency in a shared memory system wherein the shared memory system is shared by a plurality of modules, including a processing unit, and wherein the plurality of modules, including the processing unit, are coupled to a system bus, the method comprising the steps of:

causing the processing unit to cache at least some locations of the shared memory system in a cache memory;

initiating a cache coherency transaction on the system bus using one of the plurality of modules other than the processing unit; and

in response to the cache coherency transaction, causing the processing unit to execute a cache coherency operation.

10.(Original). The method of claim 9 wherein the step of initiating is performed without using an interrupt mechanism of the processing unit.

11.(Original) The method of claim 9 wherein the step of causing the processing unit to execute the cache coherency operation is performed without executing instructions on the processing unit.

12.(Previously Presented). The method of claim 9 further comprising: generating a response to the initiated cache coherency transaction using the processing unit, wherein the response is addressed to the module that initiated the cache coherency transaction and the response indicates a state of the cache memory.

13.(Previously Presented) The method of claim 9 wherein the cache coherency transaction comprises a cache flush transaction and the step of

initiating includes indicating an address in the shared memory to be flushed from the cache memory.

14.(Currently Amended) The method of claim 13 wherein the step of causing the processing unit to execute a cache coherency operation further comprises:

looking up the address in the cache;

when the lookup yields a miss, or a hit to a cache line that is unmodified with regard to ~~main~~ the shared memory system, issuing a response to the cache coherency transaction immediately;

when the lookup yields a hit to a cache line that is modified with regard to ~~main~~ the shared memory system, causing a writeback of the specified line to ~~main~~ the shared memory system followed by generating a response to the initiated transaction, wherein the response is addressed to the module that initiated the cache coherency transaction.

15.(Previously Presented) The method of claim 9 wherein the cache coherency transaction comprises a cache purge transaction and the step of initiating includes indicating an address in the shared memory to be purged from the cache memory.

16.(Currently Amended) The method of claim 15 wherein the step of causing the processing unit to execute a cache coherency operation further comprises:

looking up the address in the cache memory;

when the lookup yields a miss issuing a response to the module that initiated the cache coherency transaction;

when the lookup yields a hit to a cache line that is modified with regard to ~~main~~ the shared memory system, causing a writeback of the specified line to ~~main~~ the shared memory system followed by an invalidation of the cache line and issuing a response addressed to the module that initiated the cache coherency transaction; and

when the lookup yields a hit to a cache line that is not modified with regard to ~~main~~ the shared memory system, invalidating the cache line followed by issuing a response addressed to the module that initiated the cache coherency transaction.

17.(Currently Amended) A computing device comprising:

a transaction-based bus ~~mechanism~~ which defines a cache coherency transaction within its transaction set;

a processor coupled to the transaction based bus ~~mechanism~~;

a cache memory coupled to the processor, but not coupled directly to the transaction-based bus ~~mechanism~~; and

~~a~~ wherein the cache coherency transaction is defined within the transaction-based bus ~~mechanism~~ even when the cache memory is not coupled to the transaction-based bus ~~mechanism~~.

18.(Currently Amended) The computing device of claim 17 further comprising:

a plurality of system components other than the processor, wherein the plurality of system components are coupled to the transaction-based bus ~~mechanism~~, wherein the plurality of system components other than the processor can initiate a cache memory operation by using the cache coherency transaction defined within the transaction-based bus ~~mechanism~~, wherein the processor is configured to respond to the cache coherency transaction by treating the cache coherency transaction as an explicit command to perform a cache coherency operation.

19.(Previously Presented) The computer system of claim 1 wherein the plurality of system components other than the processor are selected from the group consisting of: an external memory interface, a PCI bridge, peripheral subsystem interface, and direct memory access controller.